

FIELD PROGRAMMABLE GATE ARRAY (FPGA) ARCHITECTURE OF DIAMOND SEARCH MOTION ESTIMATION ALGORITHM FOR REAL-TIME VIDEO APPLICATIONS

Author(s): **Muhammad Muzammil¹, Gulistan Raja², Imdad Ali³**

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Abstract:

Motion estimation (ME) is the most computationally complex part of any video codec. Various hardware architectures of ME algorithms have been proposed in the literature for fast processing. In this paper, a hardware architecture of diamond search (DS) ME algorithm has been proposed for real-time video coding of high definition (HD) 720p (1280×720) videos. The main features of the proposed architecture are reduced chip area and minimum number of clocks to calculate sum of absolute difference point which make the architecture more efficient in terms of cost and throughput. Synthesised results on Virtex4 field programmable gate array (FPGA) show that the proposed architecture can calculate the motion vectors, with both a worst case throughput of 32.14 frames/sec and the best case throughput of 145 frames/sec. Clock requirement of proposed architecture is 129.85 MHz with a power requirement of 201 mW only. Results show that the proposed architecture of DS ME algorithm is suitable for real-time HD video applications.

For full paper, contact:

Prof Muhammad Masood Rafi

Editor-in-Chief, NED University Journal of Research

Ph: +92 (21) 99261261-8 Ext:2413; Fax: +92 (21) 99261255

Email: NED-Journal@neduet.edu.pk

Website: <http://www.neduet.edu.pk/NED-Journal>



¹ Lab Engineer, Department of Electronic Engineering, International Islamic University, Pakistan, Ph. +92 (0) 51-9019610, Email: m.muzammil@iiu.edu.pk.

² Professor, Faculty of Electronics and Electrical Engineering, University of Engineering and Technology, Taxila, Pakistan, Ph. +92 (0) 51- 9047549, Email: gulistan.raja@uettaxila.edu.pk.

³ Assistant Engineer, National Centre of Physics, Quaid-e-Azam University, Pakistan, Ph. +92 (0) 51-2077300x446, Email: imali507@gmail.com.