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LVTTL IO STANDARDS AND CAPACITANCE SCALING BASED ENERGY EFFICIENT ALU DESIGN ON FPGA

Author(s): **Tanesh Kumar, Pardeep Kumar, Khalil ur Rehman Dayo, Bhawani Shankar Chowdhry, Bishwajeet Pandey**

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Abstract:
This paper presents the design for an energy efficient 64-bit arithmetic logic unit (ALU) operating in a wide range of frequencies from 125GHz -1THz. Low voltage transistor-transistor logic (LVTTL) input output (IO) standard have been used with different drive strength of 16mA, 12mA, 8mA and 4mA along with capacitance scaling from 25pF to 5pF. It is observed that on scaling down the frequency from 1THz to 125GHz, IO power is reduced up to 87.5%. Similarly, there is a significant reduction in IO power when the capacitance is scaled down from 25pF to 20pF, 15pF, and 10pF, respectively. This design is implemented on 28nm technology based Airtex-7 field programmable gate array (FPGA) device of -1 speed grade. To the best of author's knowledge, this is the first of its kind of work where an arithmetic logic unit (ALU) has been implemented using LVTTL IO standard.

For full paper, contact:
Prof Muhammad Masood Rafi
Editor-in-Chief, NED University Journal of Research
Ph: +92 (21) 99261261-8 Ext:2413; Fax: +92 (21) 99261255
Email: NED-Journal@neduet.edu.pk
Website: http://www.neduet.edu.pk/NED-Journal